TEMIC

Siliconix

SMP40P06

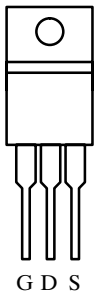
P-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

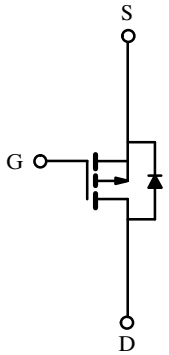
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−60	0.045	−40

TO-220AB



DRAIN connected to TAB

Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	−40	A
	T_C = 100°C		−30	
Pulsed Drain Current		I_{DM}	−100	
Avalanche Current		I_{AR}	−40	
Avalanche Energy	L = 0.1 mH	E_{AS}	90	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	45	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		62	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.2	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%.

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Specifications (T_J = 25°C Unless Otherwise Noted)

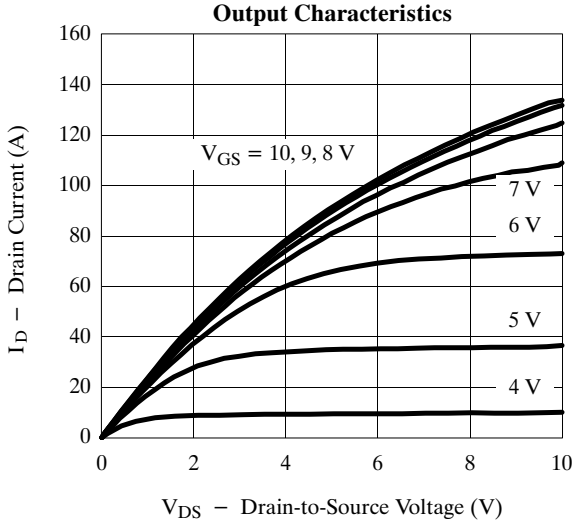
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−1		−3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −48 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 125°C			−250	
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 175°C			−500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} −10 V, I_D = −20 A		0.038	0.045	Ω
		V_{GS} = −10 V, I_D = −20 A, T_J = 125°C			0.080	
		V_{GS} = −10 V, I_D = −20 A, T_J = 175°C			0.090	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −20 A		28		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		2600		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge[c]	Q_g	V_{DS} = −30 V, V_{GS} = −10 V, I_D = −40 A		60	100	nC
Gate-Source Charge[c]	Q_{gs}			15	20	
Gate-Drain Charge[c]	Q_{gd}			17	50	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 1.5 Ω I_D ≅ −20 A, V_{GEN} = −10 V, R_G = 2.5 Ω		11	30	ns
Rise Time[c]	t_r			12	35	
Turn-Off Delay Time[c]	$t_{d(off)}$			70	140	
Fall Time[c]	t_f			75	150	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				−40	A
Pulsed Current	I_{SM}				−100	
Forward Voltage[b]	V_{SD}	I_F = −40 A, V_{GS} = 0 V		−1.2	−1.6	V
Reverse Recovery Time	t_{rr}	I_F = −40 A, dI_F/dt = 100 A/µs		81		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			7		A
Reverse Recovery Charge	Q_{rr}			0.3		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

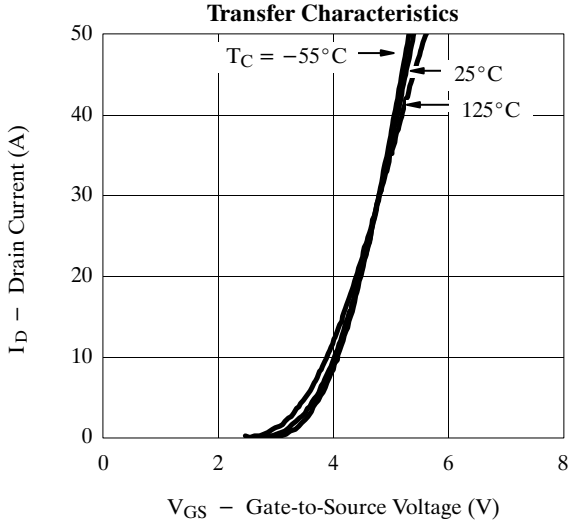
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

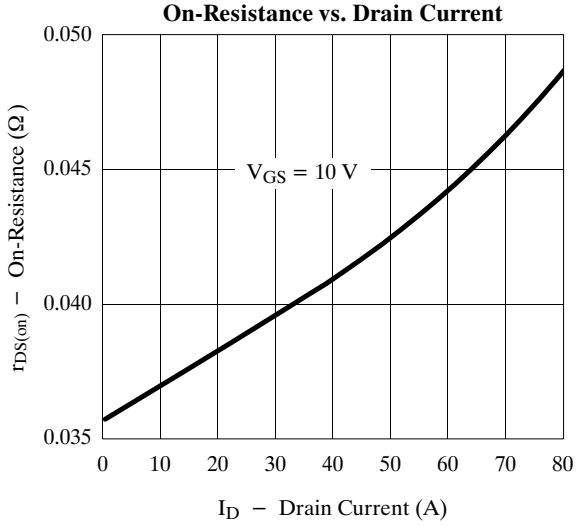
Output Characteristics



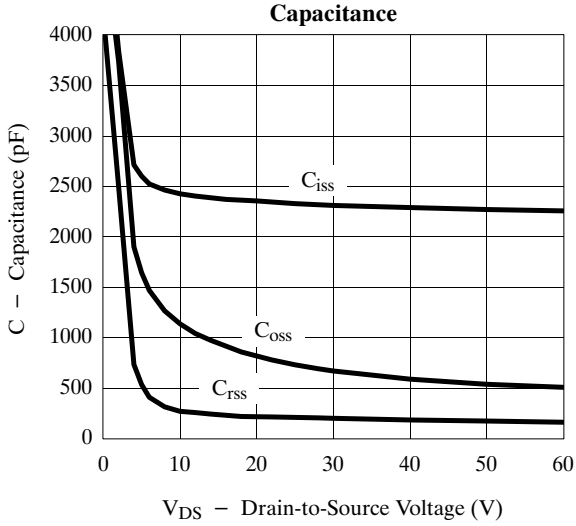
Transfer Characteristics



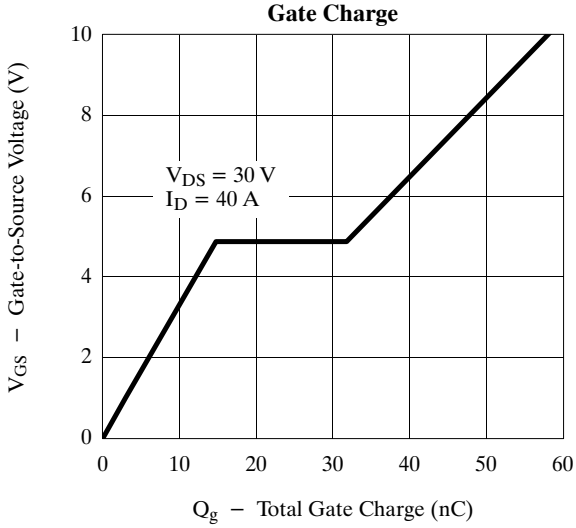
On-Resistance vs. Drain Current



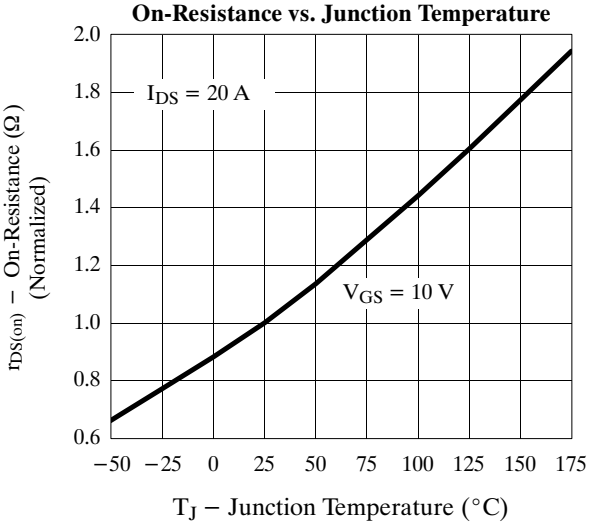
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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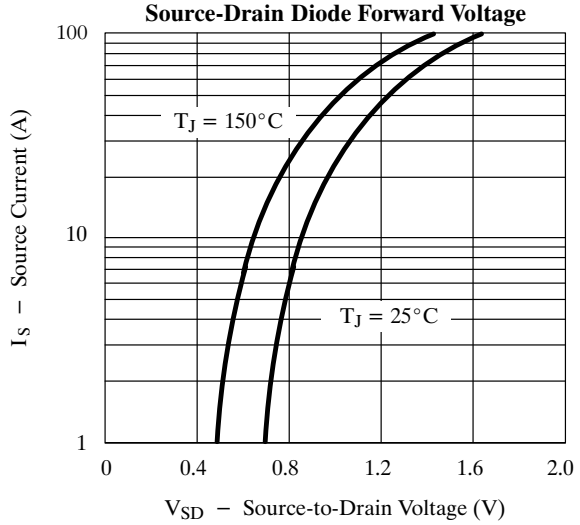
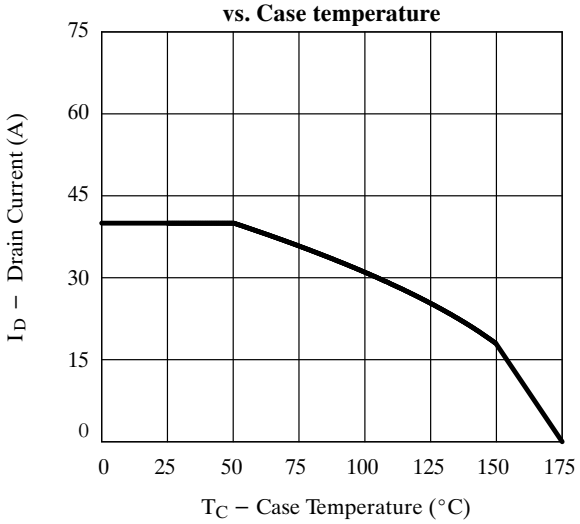
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

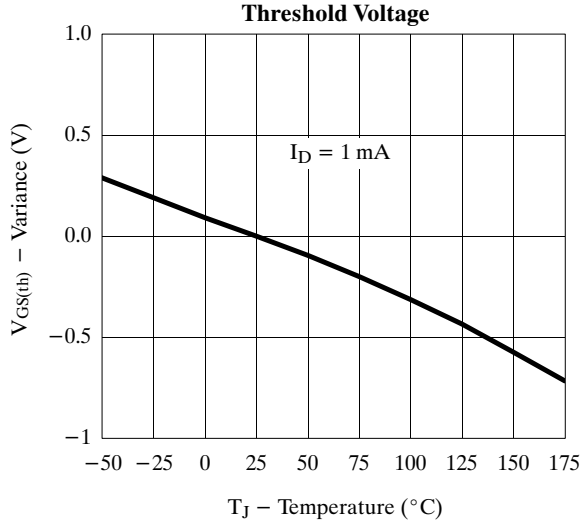
Source-Drain Diode Forward Voltage



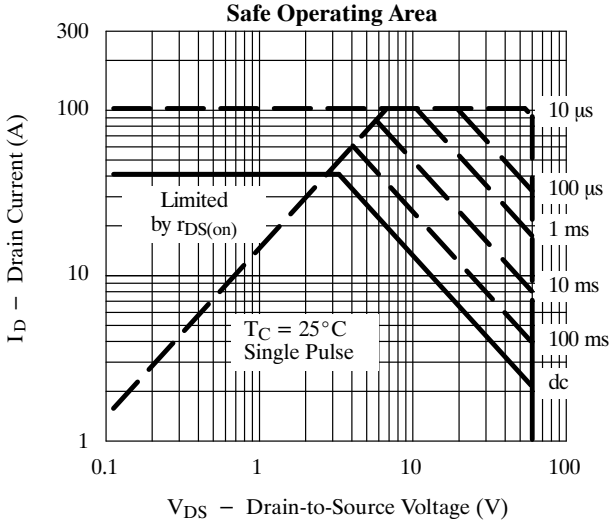
Maximum Avalanche and Drain Current vs. Case temperature



Threshold Voltage



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case